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ARCHITECTURE FOR HIGH PERFORMANCE, LOW POWER DATA CONVERTER AND FILTER, IN DEEP SUBMICRON CMOS TECHNOLOGY

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ABSTRACT:

The proposed architecture, applicable to digital communication systems, data acquisition systems and video systems. A competent general systematic automation design methodology is proposed to optimize the power because, power dissipation is a primary concern in applications requiring portability. In high frequency data converters signal were present with noise therefore we needed to process the combination of this data to filter out desired data. The proposed technique reduces the overhead of the programmer. In the proposed method, the overhead of the software developer to develop a code is minimized with the combination of data converter and filter.



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KEY WORDS: CMOS, Data converter, Filter, low power

1. Introduction

Over the past two decades, silicon integrated circuit (IC) technology has evolved so much and so quickly that the number of transistors per square millimeter has almost doubled in every eighteen months. Since the minimum channel length of transistors has been shrunk, transistors have also become faster. The evolution of IC technology has been driven mostly by the industry in digital circuits such as microprocessors and memories. As IC fabrication technology has advanced, more analog signal processing functions have been replaced by digital blocks. Despite this trend, data converters retain an important role in most modern electronic systems however; most signals of interest are analog in nature and must to be converted to digital signals for further signal processing in the digital domain.

The various data converter architectures available including flash, two-step, folding, pipeline, successive approximation and over-sampling. Each variation has unique features and which of them is deployed in specific applications is typically determined by the speed and

resolution requirements involved. The data converter architectures available, is used for low-power, medium resolution and high-speed applications, especially with CMOS technology. Nevertheless, as observed earlier, power dissipation is a primary concern in those applications requiring portability. Thus, the objective of our work is to design and build a high performing, low power data converters with filter in deep submicron CMOS technology.



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2. Review of Work

In the recent years there has been a trend in data converter research to use low accuracy analog components which are compensated for through the use of digital error correction .Because of their popularity, data converters are available in a wide variety of resolutions, sampling rates, input and output options, package styles, and costs. Many data converters now offer on-chip input multiplexers, making them the ideal choice for multichannel data acquisition system.

Pipeline ADC Linearity Testing with Dramatically Reduced Data Capture Time, has been presented a system identification based method for testing pipeline ADC's linearity. In the method, the pipeline ADC is described by an identifier model consisting of a set of nonlinear equations parameterized with some unknown parameters. The results show that this method is based on identifying the nonlinear inverse model of the pipeline ADC using a small number of I/O response points. It can cut down the data acquisition time required for full code testing by a factor of 100s to 1000s. Furthermore, it can achieve the test time reduction without adversely affecting the ADC testing accuracy. ^[2]

Low-Power Circuit Techniques for Low-Voltage Pipelined ADCs Based on Switched-Opamp Architecture: - They propose useful circuit structures for achieving a low-voltage/low-power pipelined ADC based on switched-opamp architecture. First, a novel unity-feedback-factor sample-and-hold which manipulates the features of switched-opamp technique is presented. Second, opamp-sharing is merged into switched-opamp structure with a proposed dual-output opamp configuration. A 0.8-V, 9-bit, 10-Msample/s pipelined ADC is designed to verify the proposed circuit. Simulation results using a 0.18- μ m CMOS 1P6M process demonstrate the figure-of-merit of this pipelined ADC is only 0.71 pJ/step. ^[3]



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A High Speed and High Resolution, Parallel Pipeline A/D Converter in 0.6 - μ m CMOS

The design is with a 10-bit 150MS/s CMOS parallel pipeline ADC. The converter includes four parallel interleaved pipeline A/D converters with analog background calibration using adaptive signal processing, an extra channel, and mixed signal integrators that match the offsets and gains of time interleaved ADC channels. The result shows the gain and offset mismatches of channels are reduced by adaptive background calibration. The power consumption and silicon area of time-interleaved ADC increase linearly by the number of channels. ^[4]

A low power 12-b 40-MS/s pipeline ADC has been presented a 12-bit, 40-MS/s pipelined A/D converter (ADC) which is implemented in 0.18- μ m CMOS process drawing 76-mW power from 3.3-V supply. Multi-bit architectures as well as telescopic operational transconductance amplifiers (OTAs) are adopted in all pipeline stages for good power efficiency. From the result it achieves a low frequency SFDR of over 80 dB, and preserves a 12-bit level of performance for input frequencies up to 79.1 MHz without calibration. ^[5]

A 1.8V 12-bit 230-MS/s Pipeline ADC in 0.18 μ m CMOS Technology, here they describe the implementation of a 12-bit 230 MS/s pipelined ADC using a conventional 1.8V, 0.18 μ m digital CMOS process. Two-stage folded cascade OTA topology is used for improved settling performance. Extreme low-skew (less than 3ps peak-to-peak) chip-level clock distribution is ensured by five-level balanced clock tree, implemented in low swing current-mode logic. The ADC block achieves a peak SFDR of 71.3 dB and 9.26 ENOB at 230 MS/s, with an input signal swing of 1.5Vpp. The measured peak SFDR at 200 MS/s is 78 dB, while the peak SNDR at 200 MS/s is 59.5 dB. ^[6]

Background Calibration Techniques for Multistage Pipelined ADCs with Digital Redundancy, The proposed digital background calibration scheme, applicable to multistage



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(pipelined or algorithmic/cyclic) analog-to-digital converters (ADCs), corrects the linearity errors resulting from capacitor mismatches and finite opamp gain. In the proposed method, the SNR is not degraded from the pseudorandom noise sequence injected into the system. Two-channel ADC architecture with negligible overhead is also proposed to significantly improve the efficiency of the digital correlation. This technique can correct the errors resulting from capacitor mismatches and finite opamp gain. An accurate calibration is achieved by re-calculating the digital output based on each stage's equivalent radix. ^[7]

A Hybrid Filter Bank Approach to A/D conversion, they proposed a novel approach to high-speed, high resolution Analog-to-digital (A/D) conversion using a hybrid filter bank with an array of slower speed A/D converters (ADCs). The hybrid filter bank is a new class of filter bank that employs continuous-time analysis filters to allocate a frequency band to each ADC in the array and discrete-time synthesis filters to reconstruct the digitized signal. This paper presents a filter design algorithm which minimizes mean-squared reconstruction error for the M-channel hybrid filter bank. The filter design algorithm optimizes the analog analysis filters and digital synthesis filters to cancel aliasing and compensate for ripple, non-linear phase, and imperfect implementations of the analog analysis filters to form a near-perfect-reconstruction hybrid filter bank. ^[15]

A 14-BIT 12 μ V/LSB Resolution A/D Converter For Sensors using only Digital Circuit with Low-Pass Filter Effect, A compact, high-resolution AD converter (ADC) for sensors is presented here. The basic structure is a completely digital circuit including a ring-delay line with delay units (DUs), along with a frequency counter, latch and encoder. The operating principles are, firstly, the delay time of the DU is modulated by the A/D conversion voltage; secondly, the delay pulse passes through a number of DUs within a sampling time, and the number of DUs through which the delay pulse passes is output as conversion data. In the



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expectation of the future digitalization of sensors, they have implemented an original A/D system (TAD) via a completely digital circuit for use as an A/D converter in a sensor. The TAD is compact, shrinkable and capable of high resolution. Using a prototype IC, they experimentally confirmed a 14-bit dynamic range with a resolution of 12 $\mu\text{V}/\text{LSB}$.^[16]

3. System Methodology

To design low power, high performance data converter and filter, few parameters which affect the performance of data converter and filter are,

3.1 Resolution:

The resolution of the pipeline ADC expresses the number of discrete values which can produce over the range of analog values. Electronically values are usually stored in the binary form, in order to express the resolution in the form of bits. In consequence, the number of discrete values available, or "levels", is a power of two. For example, an ADC with a resolution of 8 bits can encode an analog input to one in 256 different levels, since $2^8 = 256$. The values can represent the ranges from 0 to 255 (i.e. unsigned integer) or from -128 to 127 (i.e. signed integer), depending on the application. Number of quantization levels = 2^n

3.2 Integral Nonlinearity:

Integral nonlinearity (INL) is defined similarly to that for a DAC. Again, a "best-fit" straight line is drawn through the end points of the first and last code transition, with INL being defined as the difference between the data converter code transition points and the straight line with all other errors set to zero. Missing codes it is of interest to note the consequences of having a DNL that is equal to -1 LSB straight line drawn through the first and last output values, INL defines the linearity of the overall transfer curve and can be described as $\text{INL}_n = \text{Output value for input code } n - \text{Output value of the reference line at that point}$. The INL



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specification is measured after both static offset and gain errors have been nullified, and can be described as follows:

$INL = | [(VD - V_{zero})/V_{LSB-IDEAL}] - D |$, where $0 < D < 2^N - 1$. VD is the analog value represented by the digital output code D , N is the ADC's resolution, V_{zero} is the minimum analog input corresponding to an all-zero output code, and $V_{LSB-IDEAL}$ is the ideal spacing for two adjacent output codes.

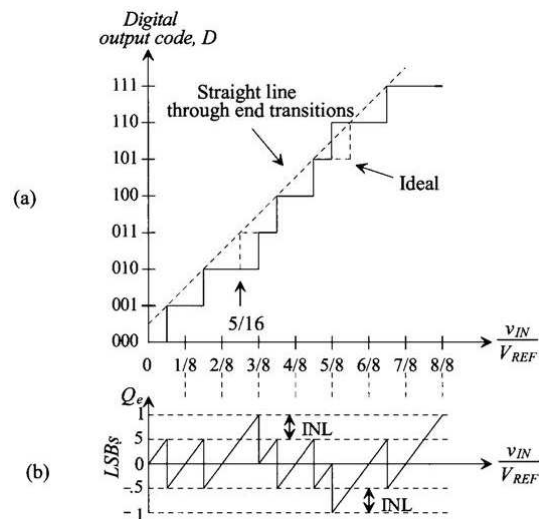


Fig 1: - (a) Transfer curve for nonideal ADC
(b) Quantization error illustrating INL

3.3 Differential Nonlinearity:

DNL is the difference between the actual code width of a nonideal converter and the ideal case. Nonideal components cause the analog increments to differ from their ideal values.



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The difference between the ideal and the nonideal values is known as Differential Nonlinearity or DNL and is defined as

$$\text{DNL} = \text{Actual step width} - \text{Ideal step width}$$

For an ideal ADC, in which the differential nonlinearity coincides with $\text{DNL} = 0\text{LSB}$, each analog step equals 1LSB ($1\text{LSB} = \text{VFSR}/2\text{N}$), where VFSR is the full-scale range and N is the resolution of the ADC and the transition values are spaced exactly 1LSB apart.

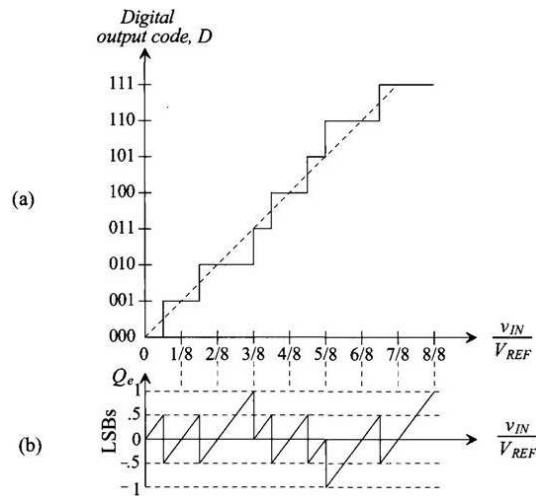


Fig 2: - (a) Transfer curve for nonideal ADC

(b) Quantization error illustrating DNL

Apart from this few more parameters which are

ENOB Chip area, bus size latency, number of taps if it is digital filter.

4. Proposed Architecture:-

There are two types of data converters ADC and DAC. We can design any one out of these two data converter or both also , following figure shows the block diagram of data



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converter with filter, here either analog or digital data, depends on types given to the data converter and o/p is taken out from the filter. One more i/p is shown to the filter to select the type of filter by giving certain coefficient values.

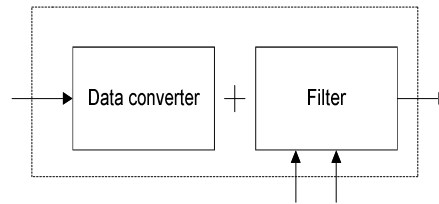


Fig 3:-

Block diagram for proposed scheme

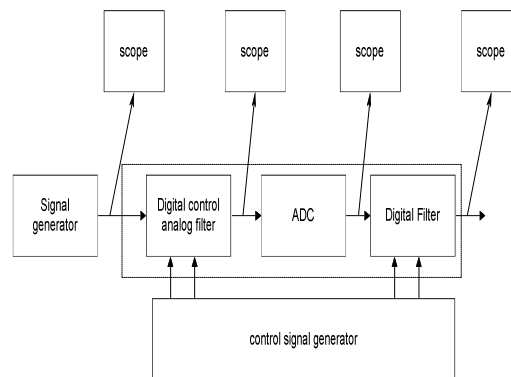


Fig 4:- Experimental setup

Above diagram shows the experimental setup for proposed design in which we use signal generator to give i/p signal to the filter and control signal generator is used to give the coefficient to select the desired filter. Here scope is used to observe the o/p of every stage to compare with our requirements.



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5. Conclusion

Architecture for high performance, low power Data Converter and filter has been proposed here. In the proposed method, the overhead of the software developer to develop a code is minimized with the combination of data converter and filter. We can also try to target the extension of measurability and observability of the device which will make the data converter and filter more powerful in terms of accuracy, resolution, and programmable features.

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